UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/064,250	04/22/1998	ELIYAHOU HARARI	HARI.006USM	5711

36257 7590 11/10/2005

PARSONS HSUE & DE RUNTZ LLP
595 MARKET STREET
SUITE 1900
SAN FRANCISCO, CA 94105

EXAMINER	
LE, VU ANH	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 11/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	09/064,250	HARARI ET AL.	
	Examiner	Art Unit	
	Vu A. Le	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *63-73* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *69-73* is/are allowed.

6)☒ Claim(s) *63-68* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/11/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 63-68 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

3. With respect to claim 63, the limitations of "***flash control buffer means for performing data exchange between the flash memory and the interface means***" and ***"access means for converting a sector address received from the external system into a substitute address and for accessing the flash memory according to the substitute address" are not supported by the specification*** (see the reason in response to arguments).

4. With respect to claim 64, the limitations of "***said flash memory includes a plurality of blocks, each block comprising an area for storing an address of***

another block and an area for storing data" and ***"said access means converts the sector address received from the external system into a substitute address and searches the block with such substitute address in order to read therefrom the number of another block*** (see the reason in response to argument).

5. With respect to claim 65, the limitations of "***the substitute address includes a logical block address***" is not supported by the specification also. In the light of the specification, the substitute address is the ***spare address*** which is different from the ***logical block address*** (see the reason in response to argument).

6. With respect to claim 66, the limitation of "***individual blocks including an area to store a block address and an area to store data***" and "***addressing circuits responsive to a sector address received through the external system interface to (a) address a corresponding block, (b) read the block address stored in the block address area of said corresponding block, and (c) if the read block address is a match, addressing another block having the address read from said corresponding block.***" ***are not supported by the specification*** (see the reason in response to arguments).

Response to Arguments

7. Applicant's arguments filed 02/04/05 have been fully considered but they are not persuasive.

8. The applicant fails to response to the rejection completely.

The limitation of "*flash control buffer means for performing* ***data exchange between the flash memory and the interface means***" in claim 63 is not supported by the specification.

9. Nowhere in the specification mentions about flash buffer means. In the recent amendment (page 6, lines 17-20), the applicant argues that "*flash control buffer means for performing* ***data exchange between the flash memory and the interface means***" is supported for example in Fig.1B, interface 40; Fig.3A, interface 227; Figs. 6 and 7, FIFO 519 and FIFO 601; Fig.8, cache 705.

This argument is found not to be persuasive since the interfaces 40 (in Fig.1B) and 227 (in Fig.3A) are not a flash buffer means and there is no "receiver 313 in Figs 6 and 7. The FIFO 519 and FIFO 601 in Figs. 6 and 7 can not be considered as a flash buffer means since these FIFOs do not perform ***data exchange between the flash memory and the interface means.*** The specification teaches that these FIFOs are used for temporarily holding read data to be shipped out of the controller in read mode (page 19, lines 6-10) and for temporarily holding write data before these data being converted to serial format and sent to the memory device 33 (page 21, lines 16-28). Because **these FIFOs are in the controller chip 31** (Figs. 1A and 1B), they perform the exchange data **between *the microprocessor 21 and the interface 40,* not *between the flash memory (43) and the interface means (40).***

The cache 705 in Fig.8 can not be considered as a flash control buffer means

also because cache 705 is used for holding the **data to be write** to flash memory array 33 only (one way transferring data), **not for reading and writting together**, so it does not perform ***data exchange*** (two way transferring data). Furthermore, cache 705 in Fig.8 are outside of the flash memory 33 and it locates **between** *the microprocessor 21 and the flash memory array 33,* **not *between the flash memory (43) and the interface means (40)*** so it can not transferring the data ***between the flash memory (43) and the interface means (40)*** as required for flash control buffer means.

10. The limitation of "*Access means for converting a sector address received from the external system into a substitute address and for accessing the flash memory according to the substitute address*" in claim 63 is not supported by the specification.

11. The applicant argues that this limitation is supported in Fig.1B, controller 31 and interface 40; Figs.2 and 3A, p.9, line 10 thorough p.11, line 6; Figs 6 and 7, p.17, line 25 through p.24, line 30.

.First of all, Fig.1B, controller 31 and interface 40 **do not show any access means** for converting a sector address into a substitute address. Fig.1B as described in the specification shows "a bulk storage memory 29 is constructed of a memory controller 31, connected to the computer system bus 23, and an array 33 of EEPROM integrated circuit chips" (page 6, lines 31-34).

.Second, Figs.2 and 3A, p.9, line 10 thorough p.11, line 6 **do not teach any thing about access means** for converting a sector address into a substitute address.

They teach about how a plurality of sectors can be erased at the same time. They teach nothing about converting a sector address and nothing about substitute address.

.Third, Figs 6 and 7, p.17, line 25 through p.24, line 30 teach "Read data path control" (Fig.6) and "Write data path control" (Fig.7) and how a defective memory cell or a defective memory sector is replaced by another alternative defect bits or sector. **They say nothing about** "*converting a sector address received from the external system into a substitute address and for accessing the flash memory according to the substitute address*".

12. The applicant argues that "It **appears** that decoding is an example of converting an address from one form (encoded) to another form (unencoded). Thus, decoding provides support for the term "converting" used in claim 63. This argument is found not to be persuasive since the term "converting" does not have the same meaning with the term "decoding". For example, converting a physical address to a logical address means changing the address from one form (physical form) to another form (logical form) while decoding an address means to recognize and interpret an address. Thus, decoding an address does not providing support for the term "converting a sector address" used in claim 63.

13. The applicant argues that "Another example of address conversion in the present application is provided by address mapping to replace ***defective sectors*** with substitute sectors. When the number in a sector exceed a predetermined value, the controller

marks that sector as defective and maps it to another sector," page 23, lines 17-19". This argument is found not to be persuasive since the mapping **happens only** when the defective sector exits. If the defective sector does not exit, the means for mapping does not perform the address conversion. In another word, when a memory sector is accessed (read or write) and **only if *that memory sector is defective***, the access will be **rerouted** to another normal memory sector. So, the condition for the mapping is the defective sector. **If there is no defective sector, there is no mapping**. While the limitation of "*Access means for converting a sector address received from the external system into a substitute address and for accessing the flash memory according to the substitute address*" in claim 63 is ***not restricted to defective sector condition*** as the means for address mapping described in the specification. "*Access means for converting a sector address received from the external system into a substitute address and for accessing the flash memory according to the substitute address*" in claim 63 will convert ***any address, no matter that address is a defective address or not.*** The address conversion as recited in claim 63 is not limited to the defective sector address as mapping in the specification. In short, the means for address mapping as described in the specification **can not** be considered as "*Access means for converting a sector address received from the external system into a substitute address and for accessing the flash memory according to the substitute address*" in claim 63 since ***such means does not convert <u>any</u> sector address when there is no defective sector*** or when the total of defective memory cells in a sector is less than the total number of memory cells in such sector.

14. With respect to claims 64 and 66, the specification fails to support the limitation of "said flash memory includes a plurality of blocks, each block comprising an area for storing an address of another block and an area for storing data." Fig.5 in specification shows a data portion (403) and defect map (407). The defect map (407) is used for storing address of the **defective cell**, not the address of **another block** (page 17, line 6-8). The specification (page 23, lines 12-31) mentions about "defect mapping of the whole sector, **but only** after the number of defective cells in the sector has exceeded the cell defect mapping's capacity for that specific sector." It means if there are few defective memory cells, the defect mapping of the whole sector does not happen. Furthermore, even if the number of defect memory cells exceeded capacity for that specific sector, the address of the replace sector is stored in another memory maintained by the controller and the memory may be located in the controller hardware. Thus, the specification fails to support the limitation of "said flash memory includes a plurality of blocks, **each block** comprising an area for storing an *address of another **block*** and an area for storing data." since the address of replace sector is stored in another memory maintained by the controller (not in a sector portion) and the defect map is used to store the address of replace memory **cell**, not address of another **block**.

15. With respect to claim 65, the applicant argues that "The Office Action stated that "the logical block address is the address for every block." However, no such limitation is recited in claim 65. Claim 65 simply recites "**the** substitute address includes **a** logical

block address." There appears to be no limitation in this claim that would limit the logical block address to being the address for every block in the semiconductor disk device. Thus, claim 65 appears to be fully supported, for example at page 23, lines 17-19, as discussed above."

Actually, the Office Action states, "With respect to claim 65, it claims "the substitute address includes a logical block address." This feature is not supported by the specification also. In the light of the specification, the substitute address is the ***spare address*** which id different from the ***logical block address. The logical block address is the address for every block in the semiconductor disk device while the spare address is not the address of every block in the semiconductor disk device***."

The explanation of why the logical block address is not supported by the specification has been **misleaded and incompletely responded** by discussing only a small part of the explanation (the logical block address is the address for every block) and **ignoring** the critical part of the explanation. The applicant **fails to response** about the silence of the specification about logical block address. In short, **nowhere in the specification mentions about the logical block address**.

Allowable Subject Matter

16. Claims 69-73 are allowed.

Conclusion

17. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vu A. Le whose telephone number is (571) 272-1871. The examiner can normally be reached on M-F (7:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vu A. Le
Primary Examiner
Art Unit 2824

11/08/05